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10/801,789	03/16/2004	Andy Yu	M-16550 US	3122

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EXAMINER	
MAI, ANH D	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,789	YU ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-11,15-17,41,44-55 and 58-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-11,15-17,41,44-55 and 58-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. The Remarks filed May 29, 2008 is acknowledged. Claims 1, 4-11, 15-17, 41, 55 and 58-68 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-8, 10 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung (U.S. Patent No. 6,018,178) of record, in view of Chang (U.S. Patent No. 5,408,115) both of record.

With respect to claim 1, Sung teaches an electrically alterable memory device substantially as claimed including:

a first semiconductor layer (2) doped with a first dopant in a first concentration;

a second semiconductor layer (3), adjacent the first semiconductor layer (2) doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer (3) having a top side; (see fig. 1);

two spaced-apart diffusion regions (14) embedded in the top side of the second semiconductor layer (3), each diffusion region (14) doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions

(14) including a first diffusion region (14aa) and a second diffusion region (14ab), and with a first channel region defined therebetween, wherein the second semiconductor layer and each diffusion region form a junction which is capable of a soft avalanche breakdown in response to a lower electrical potential imposed on the diffusion region (14) relative to the second semiconductor layer (3);

a first floating gate (10A) comprising a conductive material, the first floating gate (10A) being disposed adjacent the first diffusion region (14aa) and above the first channel region, separated therefrom by a first insulator region (9), the first floating gate (10A) capable of storing electrical charge injected into the first floating gate (10A) in response to the soft avalanche breakdown and a higher electrical potential at the first floating gate (10A) relative to the first diffusion region (14aa);

a second floating gate (10B) comprising of a conductive material, the second floating gate (10B) being disposed adjacent the second diffusion region (14ab) and above the first channel region and separated therefrom by a second insulator region (9), the second floating gate (10B) capable of storing electrical charge injected into the second floating gate (10B) in response to the soft avalanche breakdown and a higher electrical potential at the second floating gate (10B) relative to the second diffusion region (14ab); and

a control gate (5) comprising of a conductive material, the control gate (5) being disposed laterally between the first floating gate (10A) and the second floating gate (10B), the control gate (5) being separated from the first floating gate (10A) by a first vertical insulator layer (8) and being separated from the second floating gate (10B) by a

second vertical insulator layer (8), such that the first (10A) and second (10B) are each capacitively coupled to have an electrical potential derived from the electrical potential of the control gate, the control gate (5) acting as a word select line, the control gate (5) further being disposed above the first channel region without overlapping the two spaced-apart diffusion regions (14), being separated therefrom by a third insulator region (4). (See Figs. 1 and 9).

Thus, Sung is shown to teach all the features of the claim with the exception of alternatively utilizing P-type dopant for the first dopant.

However, Chang teaches that the skill in the art will recognize that while this (the n-channel EEPROM, i.e., p-well, n-type dopant regions) is by far, the most common choice for EEPROM devices, **it is also possible to reverse the conductivity and fabricate a p-channel EEPROM array**. (See col. 4, ll. 5-14).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the EEPROM of Sung to be p-channel, wherein the first dopant being p-type dopant, as taught by Chang since it is well known in the art to reverse the conductivity dopants to form the similar device, i.e., EEPROM, with difference characteristics, i.e., p-channel and n-channel and vice versa.

Regarding the limitation directing to the functionality or capability of the devices: *the second semiconductor layer and each diffusion region form a junction which is* ***capable of*** *a soft avalanche breakdown in response to a lower electrical potential imposed on the diffusion region relative to the second semiconductor layer; the first or second floating gate being* ***capable of***

storing electrical charge injected into the first or second floating gate in response to the soft avalanche breakdown and a higher electrical potential at the first or second floating gate relative to the first or second diffusion region, since the device of Sung, in view of Chang, comprises ***all*** physical limitations as claimed, therefore, the device of Sung should obviously be ***capable of*** functioning in the same manners.

With respect to claims 4 and 6, the first and second insulator region (9) of Sung have the thickness that allows tunneling of charge between the first (10A) and second (10B) floating gates and the first channel region.

With respect to claims 5 and 7, in view of Pan, the thickness of the first and second insulator region (50) are between 80 Å to 120 Å, thus, overlaps the claimed range between 70 Å and 110 Å.

With respect to claims 8 and 10, the first and second vertical insulator (8) of Sung is made from a silicon dioxide or in view of Pan, oxide-nitride-oxide (ONO) having a thickness that provides capacitance between the first floating gate (10A) and second floating gate (10B) and the control gate (5), respectively, and the first and second vertical insulator (8) prevents leakage between the first (10A) and second (10B) floating gates and the control gate (5), respectively.

With respect to claims 15, the first (10A) and second (10B) floating gate of Sung are each inherently capable of storing multiple levels of charge.

With respect to claim 16, the first (10A) and second (10B) floating gate of Sung are each inherently capable of storing four levels of charge.

With respect to claim 17, an oxide layer (9) of Sung is disposed on top of each diffusion region (14).

3. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung '178 and Chang '115 as applied to claim 1 above, and further in view of Pan (U.S. Patent No. 5,760,435) of record.

Sung and Chang teach the electrically alterable memory device as described in claim 1 above including the first and second vertical insulator layer (8) separating floating gates (10A-B) and control gate (5) and having the thickness that provides capacitance between the floating gate (10) and the control gate (5), and the insulator (8) preventing leakage between the floating gates (10A-B) and the control gate (5).

Thus, Sung is shown to teach all the features of the claim with the exception of utilizing oxide-nitride-oxide layer for the first and second vertical insulator layer (8).

However, Pan teaches that either silicon oxide or O-N-O layer can be used for the insulator layer (40) separating the floating gate (62) and control gate (30). (See col. 3, ll. 57-60).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to utilize either silicon oxide or O-N-O for the insulator of Sung as taught by Pan to preventing leakage between the floating gates and the control gate since the two materials are well known in the art to be used interchangeably.

Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of it suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416., 125 USPQ 416.

4. Claims 41-48, 50 and 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung '178 in view of Chen et al. (U.S. Patent No. 6,271,089) and Chang '115, all of record.

With respect to claim 41, Sung teaches an electrically alterable memory device substantially as claimed including:

a first semiconductor layer (2) doped with a first dopant in a first concentration;

a second semiconductor layer (3), adjacent the first semiconductor layer (2), doped with a second dopant that has an opposite electrical characteristics that the first dopant, the second semiconductor layer (3) having a top side;

two spaced-apart diffusion regions (14) embedded in the top side of the second semiconductor layer (3), each diffusion region being doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions (14) including a first diffusion region (14aa) and a second diffusion region (14ab), with a first channel region defined therebetween, wherein the second semiconductor layer (3) and each diffusion region (14) form a junction which is capable of a soft avalanche breakdown in response to a lower electrical potential imposed on the diffusion region (14) relative to the second semiconductor layer (3);

a first floating gate (10A) having a left side and a right side and comprising a conductive material, the first floating gate (10A) being disposed adjacent the first diffusion region (14aa) and above the first channel region and being separated therefrom by a first insulator region (9), the first floating gate (10A) being capable of storing electrical charge injected into the first floating gate (10A) in response to the soft

avalanche breakdown and a higher electrical potential at the first floating gate (10A) relative to the first diffusion region (14aa);

a second floating gate (10B) having a left side and a right side and comprising of a conductive material, the second floating gate (10B) being disposed adjacent the second diffusion region (14ab) and above the first channel region and being separated therefrom by a second insulator region (9), the second floating gate (10B) being capable of storing electrical charge injected into the second floating gate (10B) in response to the soft avalanche breakdown and a higher electrical potential at the second floating gate (10B) relative to the second diffusion region (14ab); and

a control gate (5) comprising of a conductive material, the control gate (5) being disposed laterally between the first (10A) and second (10B) floating gate, the control gate (5) being separated from the first floating gate (10A) by a third insulator layer (8) and being separated from the second floating gate (10B) by a fourth insulator layer (9), the control gate (5), such that the first (10A) and second (10B) floating gates are each capacitively coupled to have an electrical potential derived from the electrical potential of the control gate, the control gate further being disposed above the first channel region and separated therefrom by a third insulator region (4). (See Figs. 1 and 9).

Thus, Sung is shown to teach all the features of the claim with the exception of explicitly disclosing the control gate covering the first and second floating gate on at least right side and left side and utilizing P-type dopant for the first dopant.

However, Chen teaches the control gate (208) of electrically alterable memory device covering the first (204a) and second (204b) floating gate on at least right side and left side. (See Fig. 2B).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the control gate of the electrically alterable memory device of Sung to cover the first and second floating gates on at least right side and left side as taught by Chen to increase the numbers of bits stored in the unit area of a flash memory.

Further, Chang teaches that the skill in the art will recognize that while this (the n-channel EEPROM, i.e., p-well, n-type dopant regions) is by far, the most common choice for EEPROM devices, **it is also possible to reverse the conductivity and fabricate a p-channel EEPROM array**. (See col. 4, ll. 5-14).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the EEPROM of Sung to be p-channel, wherein the first dopant being p-type dopant, as taught by Chang since it is well known in the art to reverse the conductivity dopants to form the similar device, i.e., EEPROM, with difference characteristics, i.e., p-channel and n-channel and vice versa.

Regarding the limitation directing to the functionality or capability of the devices: *the second semiconductor layer and each diffusion region form a junction which is* ***capable of*** *a soft avalanche breakdown in response to a lower electrical potential imposed on the diffusion region relative to the second semiconductor layer; the first or second floating gate being* ***capable of***

storing electrical charge injected into the first or second floating gate in response to the soft avalanche breakdown and a higher electrical potential at the first or second floating gate relative to the first or second diffusion region, since the device of Sung, in view of Chang, comprises ***all*** physical limitations as claimed, therefore, the device of Sung should obviously be ***capable of*** functioning in the same manners.

With respect to claims 44 and 46, the first and second insulator region (9) of Sung having a thickness that allows tunneling of charge between the first and second floating gate (10) and the first channel region.

With respect to claims 45 and 47, the thickness of the first and second insulator region (9) of Sung are between 60 Å to 70 Å, thus includes lower end of the claimed range between 70 Å and 110 Å.

With respect to claims 48 and 50, the third and fourth insulator (8) of Sung or Chen are made from a silicon dioxide having a thickness that provides capacitance between the first and second floating gate (10) and the control gate (5), respectively, and wherein the third and fourth insulator (8) prevents leakage between the first and second floating gate (10) and the control gate (5), respectively.

With respect to claim 52, the first and second floating gate (10) of Sung or Chen are each inherently capable of storing multiple levels of charge.

With respect to claim 53, the first and second floating gate (10) of Sung or Chen are each inherently capable of storing four levels of charge.

With respect to claim 54, an oxide layer (9) of Sung or Chen is disposed on top of each diffusion region (14).

5. Claims 49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung '178 and Chen '089 as applied to claim 41 above, and further in view of Pan '435.

The third and fourth insulator (8) of Sung or Chen are made from a silicon dioxide having a thickness that provides capacitance between the first and second floating gate (60) and the control gate (66), respectively, and the first and second vertical insulator (64) preventing leakage between the first and second floating gate (60) and the control gate (66), respectively.

Thus, Sung and Chen are shown to teach all the features of the claim with the exception of utilize Oxide-Nitride-Oxide (ONO) for the third and fourth insulator.

However, Pan teaches ONO or silicon oxide can be used for the third and fourth insulator (40'). (See Fig. 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to use ONO for the third and fourth insulator of Sung or Chen as taught by Pan to prevents leakage between the first and second floating gates (10) and the control gate (5) since these materials are well known in the art to be used interchangeably.

Further, it has been held to be within the general skill of a worker in the art to select a known material, e.g., O-N-O, on the basis of it suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416., 125 USPQ 416.

6. Claims 55-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung '178 in view of Hong (U.S. Patent No. 5,576,232) of record and Chang '115.

With respect to claim 55, Sung teaches an electrically alterable memory device substantially as claimed including:

a first semiconductor layer (2) doped with a first dopant in a first concentration;

a second semiconductor layer (3), adjacent the first semiconductor layer (2), doped with a second dopant that has an opposite electrical characteristics than the first dopant, the second semiconductor layer (3) having a top side;

two spaced-apart diffusion regions (14) embedded in the top side of the semiconductor layer (3), each diffusion region (14) being doped with the first dopant in a second concentration, the two diffusion regions including a first diffusion region (14aa) and a second diffusion region (14ab), with a first channel region defined therebetween, wherein the second semiconductor layer (3) and each diffusion region (14) form a junction which is capable of a soft avalanche breakdown in response to a lower electrical potential imposed on the diffusion region (14) relative to the second semiconductor layer (3);

a first floating gate (10A) comprising a conductive material, the first floating gate (10A) being disposed adjacent the first diffusion region (14aa) and above the first channel region and being separated therefrom by a first insulator region (9), the first floating gate (10A) being capable of storing electrical charge injected into the first floating gate (10A) in response to the soft avalanche breakdown and a higher electrical potential at the first floating gate (10A) relative to the first diffusion region (14aa);

a second floating gate (10B) comprising a conductive material, the second floating gate (10B) being disposed adjacent the second diffusion region (14ab) and above the first channel region and being separated therefrom by a second insulator region (9), the second floating gate (10B) being capable of storing electrical charge injected into the second floating gate (10B) in response to the soft avalanche breakdown and a higher electrical potential at the second floating gate (10B) relative to the second diffusion region (14ab); and

a control gate (5) having at least two lateral sides and comprising of a conductive material, the control gate (5) being disposed laterally between the first (10A) and second (10B) floating gate, the control gate (5) being separated from the first floating gate (10A) by a first vertical insulator layer (8) and being separated from the second floating gate (10B) by a second vertical insulator layer (8), such that the first (10A) and second (10B) floating gates are each capacitively coupled to have an electrical potential derived from the electrical potential of the control gate, the control gate being separated from the first channel region by a third insulator region (4). (See Figs. 1 and 9).

Thus, Sung is shown to teach all the features of the claim with the exception of explicitly disclosing the control gate being covered by the first and second floating gates on more than one lateral side and utilizing P-type dopant for the first dopant.

However, Hong teaches the control gate (520) of the electrically alterable memory device being covered by the first floating gate (580) and second floating gate (580) on more than one lateral side. (See Fig. 7H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the control gate of the electrically alterable memory device of Sung being covered on more than one lateral side by the first and second floating gates as taught by Hong to improve device reliability.

Further, Chang teaches that the skill in the art will recognize that while this (the n-channel EEPROM, i.e., p-well, n-type dopant regions) is by far, the most common choice for EEPROM devices, **it is also possible to reverse the conductivity and fabricate a p-channel EEPROM array**. (See col. 4, ll. 5-14).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the EEPROM of Sung to be p-channel, wherein the first dopant being p-type dopant, as taught by Chang since it is well known in the art to reverse the conductivity dopants to form the similar device, i.e., EEPROM, with difference characteristics, i.e., p-channel and n-channel and vice versa.

Regarding the limitation directing to the functionality or capability of the devices: *the second semiconductor layer and each diffusion region form a junction which is* ***capable of*** *a soft avalanche breakdown in response to a lower electrical potential imposed on the diffusion region relative to the second semiconductor layer; the first or second floating gate being* ***capable of***

storing electrical charge injected into the first or second floating gate in response to the soft avalanche breakdown and a higher electrical potential at the first or second floating gate relative to the first or second diffusion region, since the device of Sung, in view of Chang, comprises ***all*** physical limitations as claimed, therefore, the device of Sung should be ***capable of*** functioning in the same manners.

With respect to claims 58 and 60, the first and second insulator region (9) of Sung or Hong has a thickness that allows tunneling of charge between the first (10A) and second (10B) floating gate and the first channel region.

With respect to claims 59 and 61, in view of Hong, the first and second insulator region (57) have the thickness of 60 Å to 100 Å, hence overlaps the claimed range between 70 Å and 110 Å.

With respect to claims 62-65, the first and second vertical insulator (8) of Sung is made from a silicon dioxide or in view of Hong, oxide-nitride-oxide (ONO) having a thickness that provides capacitance between the first floating gate (10A) and second floating gate (10B) and the control gate (5), respectively, and the first and second vertical insulator (8) prevents leakage between the first (10A) and second (10B) floating gates and the control gate (5), respectively.

With respect to claim 66, the first (10A) and second (10B) floating gates of Sung are each inherently capable of storing multiple levels of charge.

With respect to claim 67, the first (10A) and second floating gate (580) of Sung are each inherently capable of storing four levels of charge.

With respect to claim 68, an oxide layer (9) of Sung is disposed on top of each diffusion region (14).

Response to Arguments

7. Applicant's arguments filed May 29, 2008 have been fully considered but they are not persuasive.

The Declaration of Dr. Simon Wong filed May 29, 2008 has been carefully considered, however, the Declaration is not found persuasive.

With the exception of the dopant type being used, there is no structure difference between N-type and P-type EEPROM.

In the Declaration, the signer does not seem to comprehend the scope of the claims. The term "capable of..." is the functionalities or the abilities of the electrically alterable memory device. The only different between the two is P-type instead of N-type characteristics. Thus, by changing form N-type to P-type as suggested by Chang '115, the device of Sung, in view of Chang, should obviously capable of function in the soft avalanche breakdown manner.

Item 8 of the Declaration states: "**each recite a memory device that is programmed using** a soft-avalanche breakdown...".

However, the claimed invention is claiming a semiconductor device, with structural limitations, but the claims do not direct how to program a semiconductor device.

In view of Chang and also commonly known for one having ordinary skill in the art, an EEPROM can be made as either P-type or N-type.

The Declaration fails to explicitly show the structural differences between the device of Sung, in view of Chang and the claimed device.

Moreover, the support for change from N-type to P-type is suggested by the reference. Therefore the *prima facie* case of obviousness is fully established.

The rejections are therefore, maintained.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anh D. Mai/
Primary Examiner, Art Unit 2814